IN THE CLAIMS:

The following are the currently pending claims. (All claims listed)

1.-21. (Canceled)

22. (Currently Amended) An apparatus comprising:

~~a memory in a processor to store a value~~ a plurality of APIC TPR registers for each of a plurality of threads wherein execution of operating system code causes values to be stored in said registers to indicate which of ~~a~~ the plurality of threads to be executed by the processor has a higher priority;

a resource allocated between said plurality of threads depending on a priority assigned to each thread in said ~~memory~~ registers;

control logic coupled to said resource; and

a counter coupled to said control logic, wherein a value is set for each thread depending on the priority assigned to each thread, and said counter is to be loaded with one of said set values by said control logic, such that one of said threads with a higher priority is to be allocated ~~longer access to~~ a greater number of instructions processed by the resource than another of said threads with a lower priority based on a counting operation on the set value loaded into said counter, wherein said resource is selected from a group consisting of: a decode unit, a trace cache/MSROM, a rename/allocation unit, an execution unit, a retire unit, and a bus.

23. (Previously Presented) The apparatus of claim 22 wherein said counter is a down-counter, and one of said set values for a higher priority thread is greater than another of said set values for a lower priority thread.

24. (Previously Presented) The apparatus of claim 22 wherein said resource is a unit in the processor system.

25. (Previously Presented) The apparatus of claim 24 wherein said resource is a decode unit and more instructions from said thread with a higher priority are loaded into said decode unit than from one of said threads having a lower priority based on the set values loaded into said counter.

26. (Previously Presented) The apparatus of claim 24 wherein said resource is a trace cache/MSROM and more instructions from said thread with a higher priority are loaded into said trace cache/MSROM than from one of said threads having a lower priority based on the set values loaded into said counter.

27. (Previously Presented) The apparatus of claim 24 wherein said resource is a rename/allocation unit and more instructions from said thread with a higher priority are loaded into said rename/allocation unit than from one of said threads having a lower priority based on the set values loaded into said counter.

28. (Previously Presented) The apparatus of claim 24 wherein said resource is an execution unit and more instructions from said thread with a higher priority are loaded into said execution unit than from one of said threads having a lower priority based on the set values loaded into said counter.

29. (Currently Amended) The apparatus of claim 24 wherein said resource is ~~an~~ a retire unit and more instructions from said thread with a higher priority are loaded into said retire unit than from one of said threads having a lower priority based on the set values loaded into said counter.

30. (Previously Presented) The apparatus of claim 22 wherein said resource is a bus and more bus requests are serviced from said thread with a higher priority than from one of said threads having a lower priority based on the set values loaded into said counter.

31. (Cancelled)